PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
et al.

Art Unit: Unknown

Examiner: Unknown

Serial No. Unknown

Docket No. TER-002.3P D5

Filed: 1/11/01

For: **APPARATUS AND METHOD FOR SCDMA DIGITAL DATA TRANSMISSION USING ORTHOGONAL CODES AND A HEAD END MODEM WITH NO TRACKING LOOPS**

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
January 11, 2001

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above identified case as follows.

IN THE DRAWINGS

Enclosed are markups of Figures 53B and 53C to conform these figures to the description of the process given in Figure 60 and the specification changes described below with the changes marked in red. Also enclosed is a markup of Figure 60 with changes marked in red to eliminate duplicate reference numbers.

IN THE SPECIFICATION

At page 1, line 1, please delete the title and insert the following new title --

APPARATUS AND METHOD FOR TRELLIS ENCODING DATA FOR TRANSMISSION IN DIGITAL DATA TRANSMISSION SYSTEMS--

At page 143, line 26, after ".", insert --When the RU sends training data, it sets tap coefficients of its precode equalization filter such as filter 563 in Figure 33 to values that cause the precode equalization filter to not predistort the training data signal.--

At page 144, line 8, delete the sentence "The RU then sets these final tap weight coefficients into FFE and DFE equalizers within the precode equalizatin filter 563 in the transmitter of Figure 33, as symbolized by step 1124." and substitute, --To calculate the new coefficients for the precode equalization filter 563 in the RU transmitter of Figure 33, the old coefficients of the RU precode filter FFE and DFE equalization filter are convolved with the new coefficients FFE and DFE coefficients which the central unit modem symbol equalizer circuit converged on to derive new coefficients. These new coefficients are then set into the RU precode filter.--

At page 144, line 17, delete "tap weight coefficients of FFE and DFE" and substitute --the main tap of said FFE equalizer 921 in Figure 50 to one and sets the side tap coefficients of the FFE equalization filter 921 and the DFE equalization filter 929 in Figure 50 to zero --. At line 18, delete "equalizers 765 and 820, respectively to one".

At page 145, lines 10 through 13, delete the sentence "After convergence, the RU CPU reads the final tap weight coefficients for the FFE equalizer 765 and the DFE equalizer 820 via bus 833 and, in this alternative embodiment, sends these tap weight coefficients to the FFE/DFE circuit 764 in the RU receiver of Figure 30 via bus 822, as symbolized by step 1132." and substitute the following --After convergence, the RU CPU reads the final tap weight coefficients for the FFE equalizer 765 and the DFE equalizer 820 via bus 833 and calculates new tap weight coefficients for the FFE and DFE filters of the CE circuit 764 in the RU receiver of Figure 30 by convolving the old

CE filter tap weights with the FFE and DFE filter tap coefficients converged upon by the SE circuit during reception of multiple bursts of training data, and loads these newly calculated tap weight coefficients into the FFE and DFE filters of CE circuit 764 in the RU receiver of Figure 30 via bus 844, as symbolized by step 1132 of Figure 53C.--.

At page 169, line 17, delete "1502" and subsitute --1501--.

At page 169, line 21, delete "1504" and subsitute --1507--.

At page 169, line 29, delete "1506" and subsitute --1509--.

At page 169, line 31, delete "1508" and subsitute --1511--.

At page 170, line 2, delete "1510" and subsitute --1513--.

At page 170, line 10, delete "1512" and subsitute --1515--.

At page 170, line 5, delete "1516" and subsitute --1517--.

At page 170, line 12, delete "1514" and subsitute --1519--.

At page 170, line 14, after "." and before "Then", insert --The main tap coefficient of the SE feed forward equalization filter is then set to one and the side tap coefficients of the SE feed forward and decision feedback equalization filters are set to zero for receipt of payload data.--

At page 187, delete the entire paragraph that extends from line 24 to line 27.

IN THE CLAIMS

Please cancel claims 1-83 from the parent spec and add the below claims:

1. A Trellis encoder for encoding payload data bits with redundant bits and mapping the resulting bits into a constellation point, comprising:

a plurality of payload data inputs for receiving a plurality of payload bits;

a convolutional encoder having a plurality of inputs coupled directly to a

plurality of said payload data inputs and having a first output and a second output;

a separate exclusive-OR gate having an input coupled to one of said payload data inputs and having an input coupled to said first output of said convolutional encoder and having an output;

a mapper having a plurality of inputs coupled directly to a plurality of said payload data inputs, and having an input coupled to said second output of said convolutional encoder, and having an input coupled to said output of said exclusive-OR gate, and having a plurality of I outputs and a plurality of Q outputs at which signals appear which are constellation points in a quadrature amplitude modulated constellation which are derived from said payload data appearing at said payload data inputs.

2. The apparatus of claim 1 wherein said mapper functions to nonlinearly map the bits input thereto into a constellation point of a 16 QAM constellation.

3. The apparatus of claim 1 wherein three payload bits are received, and wherein said first and second payload bits are applied to said mapper in an unchanged state,, and wherein said convolutional encoder is comprised of a chain of four D type flip flops, the first, second and third of which have their outputs coupled to the input of an exclusive-OR gate which has its output coupled to the input of the next D flip flop in said chain, and the fourth flip-flop having its output coupled to an input of said mapper and to the input of said first flip flop, and wherein the exclusive-OR gate between said first and second flip flops has an input coupled to receive said second payload bit, and wherein said exclusive-OR gate between said second and third flip flops has an input coupled to

receive said first payload bit and an additional input coupled to said output of said separate exclusive-OR gate, and having an additional input coupled to the output of an AND gate which has a first input coupled to the output of said fourth flip flop and a second input coupled to the input of said fourth flip flop, and wherein said third payload bit is modified by said separate exclusive-OR gate by exclusive-OR combination with the output bit from said third flip flop of said convolutional encoder, and wherein said exclusive-OR gate having an input coupled to the output of said third flip flop and an output coupled to the input of said fourth flip flop has an additional input coupled to said output of said separate exclusive-OR gate and an additional input coupled to said output of said fourth flip flop.

4. The apparatus of claim 3 wherein said mapper has at least one control input for receiving control signals which control whether said Trellis encoder operates in a normal mode wherein one redundant bit is added to each three payload bits or a fallback mode wherein the output of said mapper is divided into two symbols and transmitted separately with the two least significant bits (y0, y1) being transmitted as first symbol or constellation point in a QPSK 4-point constellation and the two most significant bits (y3,y2) being transmitted as a second symbol or constellation in a DQPSK constellation.

5. The apparatus of claim 1 wherein said convolutional encoder and separate exclusive-OR gate are structured and coupled together to implement a 16-state convolutional encoding process which only allows certain predetermined patterns in the constellation points that are generated from said payload data bits.

6. The apparatus of claim 1 wherein said convolutional encoder and separate exclusive-OR gate are structured and coupled together so as to be characterized by parity check polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d^2_free=5.0, Nfree=1.68, and wherein the nonlinear term is given by D^2[y0(S).AND.D^(-1)y0(D)].

7. The apparatus of claim 1 wherein said mapper has multiple modes which add different numbers of redundant bits while always maintaining the code word length at 4 bits including a normal mode where one redundant bit is added per tribit, and a fallback mode which can be used when channel impairments are high wherein fewer payload bits are sent and more redundant bits are sent in each 4 bit code word.

8. An encoder for encoding payload data bits with redundant bits and mapping the resulting bits into a constellation point so as to achieve a coding gain, comprising:

first means for receiving a plurality of payload data bits and convolutionally encoding said payload bits to generate at least one additional bit derived mathematically from a Boolean logic combination of said payload bits, and for outputting at least some of said payload bits unchanged and at least one of said payload bits as modified by a logical operation with a bit output from an intermediate stage of a convolutional encoding process carried out in said first means, and outputting a final bit resulting from said convolutional encoding process; and

second means coupled to receive one or more mode control signals and coupled to receive said final bit from said convolutional encoding process and said

unchanged payload bits and said payload bit after modification by said convolutional encoding process, for mapping said bits into a constellation point of a constellation of possible data points, each point defined by a value on a real axis and a value on an imaginary axis, said mapping having at least a normal mode and a fallback mode .

9. The encoder of claim 8 wherein said first means includes a 16-state convolutional encoder characterized by parity check polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d^2_free=5.0, Nfree=1.68 and wherein the nonlinear term is given by D^2[y0(S).AND.D^(-1)y0(D)].

10. The encoder of claim 8 wherein said first means and second means implement a forward error correction encoder state machine or lookup table coupled to a state memory which adds at least one extra bit to provide redundancy for error detection and correction and for use by a Viterbi Decoder in a receiver for ascertaining with greater accuracy the data that was actually sent despite the presence of noise, said at least one extra bit providing a constellation that is bigger than the constellation would have without said extra bit(s) thereby enabling more spacing between constellation points thereby enabling better discrimination between points by the receiver and lowering the bit error rate without increasing the bandwidth.

11. A process for Trellis encoding a plurality of payload bits into a constellation point, comprising:

receiving a plurality of payload bits;

convolutionally encoding a combination of said payload bits into one or more additional bits by applying said payload bits to different inputs of a convolutional encoder and also applying a modified bit to an input of said convolutional encoder, said modified bit being generated by exclusive-ORing one of said payload bits with an output bit from an intermediate stage of said convolutional encoder, said convolutional encoding step resulting in output of one or more additional bits; and

mapping the combination of at least some of said payload bits in an unmodified state, said modified bit and said one or more additional bits into a constellation point.

12. The process of claim 11 wherein said process for Trellis encoding is performed upon multiple pluralities of said payload bits successively, and wherein said step of convolutionally encoding comprises introducing a certain dependency between successive constellation points generated from said successive plurality of payload bits such that only certain patterns or permissible sequences of constellation points are permitted, said patterns or permissible sequences capable of being modelled in a receiver's Viterbi decoder as a Trellis code.

13. The process of claim 11 wherein said step of mapping includes the steps of receiving a control signal that indicates whether a normal mode or a fallback mode is to be implemented wherein said normal mode maps said plurality of payload bits, said modified bit and said one or more additional bits into a constellation point in a constellation of points that is larger than a constellation of possible points would be if

only the original payload bits were mapped into a constellation, and said fallback mode mapping said plurality of payload bits in an unmodified state, said modified bit and said one or more additional bits into a constellation point in a constellation of points that is larger than the constellation of points that are possible in said normal mode.

14. The process of claim 11 wherein the step of convolutionally encoding is characterized by parity check polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d^2_free=5.0, Nfree=1.68, and wherein the nonlinear term is given by D^2[y0(S).AND.D^(-1)y0(D)].

REMARKS

The amendment to page 143, line 26 is made to make clear that which would be apparent to one skilled in the art as inherently necessary in an upstream training process where tap coefficients of a central unit modem are trained and later sent down to the RU transmitter to be used there to calculate new RU precoder filter tap coefficients so as to predistort the transmitted signal so that it will arrive already equalized. Since step 1126 of Figure 53B teaches setting the coefficients of the central unit modem symbol equalizer circuit to one after transferring the converged coefficients to the remote unit transmitter, one skilled in the art would understand that the central unit modem is not equalizing, so the remote unit must be doing the equalizing for its particular signal path for that is the reason for the transfer of the converged coefficients back down to the RU. Therefore, it would be necessary during the convergence process for the RU transmitter to not predistort the equalization training

data in some embodiments, and one skilled in the art would understand this. Obviously, after the transfer of the SE converged coefficients from the CU SE circuit to the RU precode filter, the RU precode filter is doing the equalization for this RU, and it is necessary to set the CU SE filter coefficients to values which render it transparent so as to not goof up the equalization being performed by the RU precode filter. Further, the software appendices of the parent case, U.S. patent application entitled "APPARATUS AND METHOD FOR SCDMA DIGITAL DATA TRANSMISSION USING ORTHOGONAL CODES AND A HEAD END MODEM WITH NO TRACKING LOOPS", serial number 08/895,612, filed 7/16/97, define a system with remote unit and central unit modems that act in this way. This amendment should not raise new matter issues, but if the Examiner disagrees, the courtesy of a telephone call to the undersigned is respectfully requested.

The same comments apply to the amendment to page 144, line 17 with the additional comment that one skilled in the art of equalization in distributed digital data transmission systems would realize that it was an error to say that all the taps of the FFE and DFE equalization filters are set to one after convergence and transfer of the converged tap coefficients to the RU since this is an obvious error. One skilled in the art would realize that only the main tap of the FFE is set to one and the side taps of the FFE and DFE are set to zero to receieve payload data.

The amendment at page 144, line 8 conforms the description of step 1124 in the upstream equalization process embodiment of Figure 53B for the CDMA specific transmitters disclosed herein to step 1514 of the process of Figure 60 which is an equalization process which is useful in any distributed digital data system with multiple transmitters transmitting to a singe central unit transmitter over different paths regardless of the type of multiplexing in use. Those skilled in the equalization art would

realize that the original description of step 1124 was erroneous in not mentioning convolving the old coefficients with the new coefficients. Further, the software appendices of the parent case, U.S. patent application entitled "APPARATUS AND METHOD FOR SCDMA DIGITAL DATA TRANSMISSION USING ORTHOGONAL CODES AND A HEAD END MODEM WITH NO TRACKING LOOPS", serial number 08/895,612, filed 7/16/97, define a system with remote unit and central unit modems that act in this way. This amendment should not raise new matter issues, but if the Examiner disagrees, the courtesy of a telephone call to the undersigned is respectfully requested.

The change to page 145, lines 10-13 is made to correct an error that persons skilled in the art of equalization would have readily understood was made in the description of how the new CE equalization circuit coefficients are calculated after convergence of the SE coefficients. Persons skilled in the art would appreciate that the new RU receiver SE coefficients cannot be loaded directly into the RU CE equalizer circuit but must, instead, be convolved with the old CE circuit coefficients to generate the new CE coefficients. Further, this amendment conforms the description of the process of Figure 53C to the process described in Figure 60 and the accompanying text. Further, the software appendices of the parent case, U.S. patent application entitled "APPARATUS AND METHOD FOR SCDMA DIGITAL DATA TRANSMISSION USING ORTHOGONAL CODES AND A HEAD END MODEM WITH NO TRACKING LOOPS", serial number 08/895,612, filed 7/16/97, define a system with remote unit and central unit modems that act in this way. This amendment should not raise new matter issues, but if the Examiner disagrees, the courtesy of a telephone call to the undersigned is respectfully requested.

The same comments made regarding the change to page 143, line 26 apply to the

change made to page 170, line 14 since a person skilled in the art would realize that after the CU SE filter coefficients have converged and its coefficients have been sent to the RU to generate new precode filter coefficients there by convolving with the old coefficients of the precode filter, it is necessary to set the SE coefficients in the CU receiver to values such that the CU SE does not screw up the equalization now being performed by the RU precode filter. Those skilled in this art know that those tap coefficients are one for the SE FFE main tap and zero for the SE FFE and DFE side taps. No new matter is believed to be raised by this amendment.

The changes to pages 169 and 170 simply correct duplicate reference numbers which refer to different process steps.

The change to page 170, line 14 simply corrects an error which would have been detected by persons skilled in the art of equalization. After the coefficients of the SE circuit have converged and have been convolved with the old CE coefficients to derive new CE coefficients, the SE coefficients must be set to main tap = 1 and side taps = 0 since to not do so would result in the equalization being done in the RU precode filter in the case of upstream transmissions or the RU CE circuit in the case of downstream transmissions being screwed up by the SE circuit in the RU. Persons skilled in the art appreciate that after the new precode or CE coefficients have been set, the SE coefficients need to be set to a transparent state of main tap = 1 and side taps = 0 so that the SE circuit is

transparent (and can start to reconverge on subsequent iterations or periodic updates of the precode or CE coefficients).

Respectfully submitted,

Dated: January 11, 2001

Ronald Craig Fish
Reg. No. 28,843
Tel 408 778 3624
FAX 408 776 0426
Ronfpatents@worldnet.att.net

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231
on 1/12/2001
(Date of Deposit)

Ronald Craig Fish, President
Ronald Craig Fish, a Law Corporation
Reg. No. 28,843